SUMMARY OF THE CLAIMS

Claims 1-6 (withdrawn)

Claim 7. (currently amended) A method of producing a semiconductor apparatus, the method comprising the steps of:

forming metal ball bumps in direct contact with a circuit pattern of a semiconductor device formed on a semiconductor substrate in a semiconductor wafer state~~,~~;

forming a resin film on a circuit pattern forming surface of said semiconductor device so as to seal spaces between said metal ball bumps and to become thinner than a height of the metal ball bumps;

cleaning the surfaces of the metal ball bumps projecting out from the resin film;

after the cleaning step, forming solder layers different in composition from the metal ball bumps on the surfaces of the metal ball bumps;

after the forming solder layers step, cutting the semiconductor substrate into unit semiconductor chips, each semiconductor chip having at least one of said semiconductor device; and

after the cutting step, mounting at least one of the semiconductor chips on a mounting board from a bump forming surface side of the semiconductor chip so as to connect the solder layers of the semiconductor chip to the mounting board ~~at the bumps~~ with the resin film directly contacting the semiconductor chip and not directly contacting the mounting board ~~without the use of a resin formed between and contacting both the semiconductor chip and the mounting board~~.

Claim 8. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the surfaces are cleaned by removing components inviting a rise in a connection resistance and a decline in a joint strength at least at a connection interface.

Claim 9. (canceled)

Claim 10. (previously presented) A process of production of the semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, any resin film components deposited on said bumps are removed.

Claim 11. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, oxides on said bump surfaces are removed.

Claim 12. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed by plasma cleaning.

Claim 13. (original) A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least sputter etching by discharge plasma of an inert gas.

Claim 14. (original) A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of an inert gas.

Claim 15. (original) A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of a reducing gas.

Claim 16. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed by irradiating a laser beam.

Claim 17. (currently amended) A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said ~~third~~ cleaning step, the cleaning of the surfaces of the bumps is performed under a reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere.

Claim 18. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said cleaning step, the cleaning of the surfaces of the bumps is performed while applying a gas jet to the bumps to peel off the unnecessary components which are then sucked away.

Claim 19. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 7, wherein

the metal bumps formed in the first step are solder bumps.

Claim 20. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 19, wherein said solder bumps have a melting point higher than a melting point of said solder layers and said solder layers are comprised of a eutectic solder.

Claim 21. (previously presented) A process of production of a semiconductor apparatus as set forth in claim 20, wherein, in said forming solder layers step, the eutectic solder layers are formed by a printing method, plating method, or transfer method.

Claims 22-24. (canceled)

REMARKS

Claims 1-8 and 10-21 are pending in the application. Claims 1-6 are withdrawn from consideration as being directed to non-elected inventions. In the Final Office Action of June 27, 2003, the Examiner made the following disposition:

A.) Rejected claims 7, 8 and 10-21 under 35 U.S.C. §112, first paragraph.

B.) Rejected claim 17 under 35 U.S.C. §112, second paragraph.

C.) Rejected claims 7, 8, 10, 11, 16, and 19-21 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Hotchkiss* and *Behun*.

D.) Rejected claims 12, 13, and 17 under 35 U.S.C. §103(a) as being unpatentable over *Hayes, Hotchkiss* and *Behun*, and further in view of *Nishikawa et al.* and *Denning et al.*

E.) Rejected claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over *Hayes*, *Hotchkiss*, *Behun*, *Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura*.

F.) Rejected claim 18 under 35 U.S.C. §103(a) as being unpatentable over *Hayes*, *Hotchkiss* and *Behun*, and further in view of *Jackson*.

Applicant respectfully traverses the rejections and addresses the Examiner's disposition as follows:

A.) Rejection of claims 7, 8 and 10-21 under 35 U.S.C. §112, first paragraph:

Claim 7 has been amended as per the Examiner's request to overcome the rejection.

Claims 8 and 10-21 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

B.) Rejection of claim 17 under 35 U.S.C. §112, second paragraph:

Claim 17 has been amended as per the Examiner's request to overcome the rejection.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

C.) Rejection of claims 7, 8, 10, 11, 16, and 19-21 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Hotchkiss* and *Behun*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7, as amended, claims a metal ball bump having a solder layer formed thereon, wherein the solder layer is mounted to a mounting board.

This is unlike *Hayes* in view of *Hotchkiss* and *Behun*, none of which disclose or suggest a metal ball bump having a solder layer formed thereon, with the solder layer mounted to a mounting board. Unlike Applicant's claim 7, *Hayes* fails to disclose a metal ball bump having a solder layer formed thereon. Instead, *Hayes* discloses a solder column 3 having a metal ball bump 9 formed thereon. *Hotchkiss* discloses a metal ball bump 114 with no solder layer formed thereon. And *Behun* discloses an LMP solder 16 having a HMP metal ball bump 18 formed thereon.

Therefore, unlike Applicant's claim 7, none of the cited references, taken alone or in combination, disclose or suggest a metal ball bump having a solder layer formed thereon. Accordingly, *Hayes* in view of *Hotchkiss* and *Behun* fails to disclose or suggest claim 7.

Further, the method disclosed in claim 7 is beneficially simpler than the Examiner's method allegedly suggested by the combination of *Hayes*, *Hotchkiss*, and *Behun*. It is simpler to form a solder layer on a metal ball bump, as in Applicant's claimed method, than to form a metal ball bump on a solder column or LMP solder, as in the cited references. For example, in *Hayes*, solder columns 3 must be formed before forming solder balls 9, which requires additional processing steps for forming the cavities into which the solder columns 3 are formed. And in *Behun*, HMP solder balls 18 must be formed and maintained prior to being placed on the LMP solder 16 and the LMP solder 16 being reheated for wetting to the HMP solder balls 18.

Thus, for at least this additional reason, *Hayes* in view of *Hotchkiss* and *Behun* fails to disclose or suggest Applicant's claim 7.

Claims 8, 10, 11, 16, and 19-21 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

D.) Rejection of claims 12, 13, and 17 under 35 U.S.C. §103(a) as being unpatentable over *Hayes, Hotchkiss* and *Behun*, and further in view of *Nishikawa et al.* and *Denning et al.*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes, Hotchkiss* and *Behun* as discussed above. *Nishikawa* and *Denning* still fail to disclose or suggest a metal ball bump having a solder layer formed thereon, with the solder layer mounted to a mounting board. Therefore, *Hayes, Hotchkiss* and *Behun*, and further in view of *Nishikawa* and *Denning* still fails to disclose or suggest Applicant's claim 7.

Claims 12, 13 and 17 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

E.) Rejection of claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over *Hayes, Hotchkiss, Behun, Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes, Hotchkiss, Behun, Nishikawa*, and *Denning* as discussed above. *Okumura* still fail to disclose or suggest a metal ball bump having a solder layer formed thereon, with the solder layer mounted to a mounting board. Therefore, *Hayes, Hotchkiss, Behun, Nishikawa*, and *Denning,* and further in view of *Okumura* still fails to disclose or suggest Applicant's claim 7.

Claims 14 and 15 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

F.) Rejection of claim 18 under 35 U.S.C. §103(a) as being unpatentable over *Hayes, Hotchkiss* and *Behun*, and further in view of *Jackson*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes, Hotchkiss* and *Behun* as discussed above. *Jackson* still fail to disclose or suggest a metal ball bump having a solder layer formed thereon, with the solder layer mounted to a mounting board. Therefore, *Hayes, Hotchkiss* and *Behun*, and further in view of *Jackson* still fails to disclose or suggest Applicant's claim 7.

Claim 18 depends directly or indirectly from claim 7 and is therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 7-8 and 10-21 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

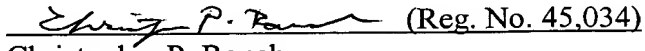
Respectfully submitted,

(Reg. No. 45,034)

Christopher P. Rauch
SONNENSCHEIN, NATH & ROSENTHAL LLP
P.O. Box #061080
Wacker Drive Station - Sears Tower
Chicago, IL 60606-1080
Telephone 312/876-2606
Customer #26263
Attorneys for Applicant(s)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 29, 2003.

 (Reg. No. 45,034)

Christopher P. Rauch